

HALF-BRIDGE CIRCUIT

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Background of the Invention:Field of the Invention:

The present invention relates to a half-bridge circuit having a first and a second transistor that are connected in series, and having a drive circuit for driving the transistors. The invention relates, in particular, to a half-bridge circuit for use in a switching regulator.

The handbook "1999/2000 Industrial Power Seminar", pages 6-3 and 6-7, from Intersil Corporation™, Irvine, CA USA 92618, describes a switching regulator with a half-bridge circuit as shown in Fig. 1. The half-bridge circuit shown in Fig. 1 has two n-channel MOSFETs M1, M2, whose drain-source paths are connected to form a series circuit. This series circuit is connected to a supply voltage U1. A drive circuit 100 is provided for driving the MOSFETs M1, M2. The drive circuit 100 is connected to the gate connections of the MOSFETs M1, M2 and to the supply voltage for voltage supply purposes. So that the required drive potential for the first MOSFET M1, which functions as a high-side switch, can be made available in the drive circuit 100, a bootstrap circuit with a capacitor C2 and

a diode D1 is provided, which is likewise connected to the drive circuit 100. The drive potential required for the first MOSFET M1 is higher than the supply voltage U1.

5 The known half-bridge circuit shown in Fig. 1 is part of a switching regulator, a so-called buck converter in the example illustrated, which provides a smaller output voltage U2 from the supply voltage U1. In this case, a series circuit including a coil L1 and a capacitor C1 is connected in parallel with the second MOSFET M2, which functions as a low-side switch. It is possible to tap off the output voltage U2 across the capacitor C1.

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20 Switching regulators of this type are used, in particular, in computers for supplying voltage to the CPU. In this case, the input voltage is usually 5.0 V and the output voltage is between 1.3 V and 2.0 V. A customary clock frequency with which the two MOSFETs are switched is about 200 kHz. In this case, the two MOSFETs M1, M2 are driven, depending on the output voltage U2, such that the output voltage is at least approximately constant - independently of the load and of fluctuations in the input voltage.

For future applications in computers, the switching regulators
25 ought to be able to correct a load change at the output of the switching regulator within a time period of less than 100 ns.

That requires clock frequencies of 2 MHz or more for the switches.

In this case, the line connections between the components and the half-bridge should be as short as possible. Furthermore, the two transistors should be accommodated in one housing, as much as possible, to save space.

In the case of the known half-bridge circuit, a comparatively high outlay is required to accommodate the two transistors and possibly also the drive circuit. Vertically designed transistors are usually used as the power transistors in switching regulators. Such transistors are usually applied to a printed circuit board by their rear side, which forms the drain connection of the transistor. In the case of the known circuit arrangement shown in Fig. 1, different potentials are required at the drain connections of the transistors, so that a printed circuit board on which the two transistors are to be jointly applied must have at least two islands with different potentials. Moreover, if the intention is to accommodate the drive circuit on the same printed circuit board, at least three such potential islands must be provided.

Summary of the Invention:

It is accordingly an object of the invention to provide a half-bridge circuit which overcomes the above-mentioned disadvantages of the prior art apparatus of this general type.

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In particular, it is an object of the invention to provide a half-bridge circuit for switching regulators, which can be realized in a space-saving manner and which can be used at comparatively high switching frequencies.

With the foregoing and other objects in view there is provided, in accordance with the invention, a half-bridge circuit including a first semiconductor body having a first MOS transistor that is integrated in the first semiconductor body. The first MOS transistor is a vertically designed n-conducting MOS transistor. The half-bridge circuit includes a second semiconductor body having a second MOS transistor that is integrated in the second semiconductor body. The second MOS transistor is a vertically designed p-conducting MOS transistor. The half-bridge circuit also includes: a drive circuit for driving the first MOS transistor and the second MOS transistor; a common connection plate to which the first MOS transistor and the second MOS transistor are applied; and a first connection terminal and a second connection terminal.

The first MOS transistor and the second MOS transistor are

connected in series between the first connection terminal and the second connection terminal.

In accordance with an added feature of the invention, the first semiconductor body has a front side and a rear side; the first MOS transistor has a drive connection and a first load path connection that are accessible at the front side of the first semiconductor body; the first MOS transistor has a second load path connection that is accessible at the rear side of the first semiconductor body; the second semiconductor body has a front side and a rear side; the second MOS transistor has a drive connection and a first load path connection that are accessible at the front side of the second semiconductor body; and the second MOS transistor has a second load path connection that is accessible at the rear side of the second semiconductor body.

In accordance with an additional feature of the invention, a capacitor is connected between the first load path connection of the first transistor and the first load path connection of the second transistor.

In accordance with another feature of the invention, the capacitor is applied to the first semiconductor body and to second semiconductor body; the capacitor has a first connection connected to the first semiconductor body; and the capacitor has a second connection connected to the second semiconductor body.

In accordance with a further feature of the invention, a bonding wire electrically connects the first connection of the capacitor to the first semiconductor body; and a bonding wire
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In accordance with yet a further feature of the invention, a common housing surrounds the first semiconductor body, the second semiconductor body, and the drive circuit.

5 The invention makes use of the fact that in a half-bridge circuit with a p-conducting transistor and an n-conducting transistor, of which only one at a time is to be driven conductively, the drain connections of the two transistors are connected to one another and are thus at a common potential. The rear sides of the two semiconductor bodies in which the two transistors are integrated can thus be applied to a common electrically conductive connection plate. The respective drain connection is accessible at each of the rear sides. This connection plate is, in particular, a lead frame of a housing for integrated circuits. The source connections and the gate connections of the transistors are available for further interconnection at the respective front sides of the semiconductor bodies.

20 In the half-bridge circuit, the first p-conducting transistor and the second n-conducting transistor are connected in series between a first terminal for a first supply potential and a second terminal for a second supply potential. The integrated drain connections of the two transistors form the output of the half-bridge circuit in this case. In the case of the customary interconnection of the half-bridge circuit, a

positive supply potential is present at the first connection terminal and a negative supply potential, or ground, is present at the second connection terminal. The p-channel transistor then functions as a high-side switch and the n-channel transistor functions as a low-side switch. Using a p-channel transistor as a high-side switch in the circuit arrangement provides the advantage that there is no need for a bootstrap circuit for providing an increased drive potential for the high-side switch.

The on resistance of a p-channel transistor is greater than that of an n-channel transistor having the same channel cross-sectional area. In the present invention, using a p-channel transistor does not constitute a disadvantage with regard to future expected applications. In future switching regulators, it is expected that the ratio of the input voltage to the output voltage will increase further. In present switching regulators with an input voltage of 5 V and an output voltage of about 1.2 V, this ratio is about 4.17. In switching regulators for future applications, in particular, in switching regulators for supplying voltage to a CPU in a computer, a ratio of the input voltage to the output voltage of 10 or more can be expected. In so-called buck converters, which provide a smaller output voltage from an input voltage, the relationship between the time duration during which a current flows via the high-side switch and the duration of a

clock period is like the relationship between the output voltage and the input voltage. Given a ratio of input voltage to output voltage of 10, current flows through the p-channel transistor as the high-side switch only about 10% of the time, while a current flows via the low-side switch over 90% of the time. To better dissipate the heat loss to the outside, it is desirable for the power loss to be distributed uniformly between the two transistors. Since the low-side switch conducts nine times as long as the high-side switch, the resistance of the low-side switch is permitted to be only $1/9$ of the resistance of the high-side switch if the same power loss is obtained on both transistors. In other words: the resistance of the high-side switch is permitted to be nine times as large as the resistance of the low-side switch. The costs and the space requirement of a p-channel transistor which is used as high-side switch and whose on resistance is nine times as large as the on resistance of the associated n-channel transistor used as low-side switch are likely to be lower than those of the low-side switch.

Moreover, by dispensing with the bootstrap circuit, the half-bridge circuit can be realized in a space-saving and cost-effective manner. This holds true all the more as the capacitor of the bootstrap circuit is usually embodied as an external component, which particularly affects the costs in the case of conventional half-bridge circuits.

One embodiment of the invention provides for a capacitor to be connected between the source connection of the first transistor and the source connection of the second transistor, that is to say in parallel with the supply terminals. This capacitor serves for bridging switching spikes that can arise during the clocked driving of the two transistors. The capacitance of this capacitor can be comparatively small at high switching frequencies. Therefore, one embodiment of the invention provides for a first connection of this capacitor to be directly connected to the source connection at the front side of the first semiconductor body of the first transistor, and for the other connection of the capacitor to be connected directly to the source connection at the front side of the semiconductor body of the second transistor. The connection between the capacitor and the source connections is preferably effected by bonding wires or by directly soldering or bonding the capacitor connections onto the source connections. The capacitor is, in particular, a ceramic capacitor that has an elongate form and an exposed connection at each of the ends. An insulating ceramic layer covers the remainder of the capacitor.

A further embodiment of the invention provides for the drive circuit to be integrated in a third semiconductor body which is applied directly to the source connection at the front side

of the semiconductor body of the n-conducting second transistor.

The two transistors, the drive circuit and, if appropriate, the capacitor of the half-bridge circuit can in this way be accommodated in a housing in a space-saving manner.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a half-bridge circuit, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 shows a prior art half-bridge circuit;

Fig. 2 shows an electrical equivalent circuit diagram of an inventive half-bridge circuit;

Fig. 3a shows a plan view of an inventive half-bridge circuit with a first transistor and a second transistor on a common connection plate;

Fig. 3b is a sectional illustration of the half-bridge circuit shown in Fig. 3a;

Fig. 4a is a plan view of an inventive half-bridge circuit with a drive circuit applied to the semiconductor body of the first transistor;

Fig. 4b is sectional illustration of the half-bridge circuit with the drive circuit shown in Fig. 4a;

Fig. 4c is sectional illustration of another embodiment of the half-bridge circuit with the drive circuit shown in Fig. 4a;

Fig. 5 shows an electrical equivalent circuit diagram of another embodiment of the half-bridge circuit;

Fig. 6a shows a plan view of the half-bridge circuit shown in Fig. 5, which is applied to a common connection plate; and

Fig. 6b shows a sectional illustration of the half-bridge circuit shown in Fig. 6a.

Description of the Preferred Embodiments:

- 5 Referring now to the figures of the drawing in detail and first, particularly, to Fig. 2 thereof, there is shown the electrical circuit diagram of an inventive half-bridge circuit. The circuit arrangement has a p-channel transistor P and an n-channel transistor N, which are each designed as vertical power MOSFETs. The transistors P and N are connected in series between a first terminal K1 and a second terminal K2. An input voltage U_{in} can be applied between the first terminal K1 and the second terminal K2. The source connection SP of the p-channel transistor P is connected to the first terminal K1 and the source connection SN of the n-channel transistor N is connected to the second terminal K2. The interconnected drain connections DP, DN of the two transistors P, N form an output OUT of the half-bridge circuit.
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- 20 A drive circuit 10 having supply connections 102, 103 is provided for driving the two transistors P, N. The supply connection 102 is connected to the first terminal K1 and the supply connection 103 is connected to the second terminal K2. The gate connection GP of the p-channel transistor P is
- 25 connected to a first output 104 of the drive circuit 10. The gate connection GN of the n-channel transistor N is connected to a second output 105 of the drive circuit 10. The two

transistors P, N are driven via the outputs 104, 105 of the drive circuit 10 according to a drive signal S_{in} that is present at an input 101 of the drive circuit 10. In this case, the two transistors P, N are driven such that only one of the two transistors P, N is in the on state so that the two connection terminals K1, K2 are never short-circuited.

In order to provide a better understanding of the mode of operation and the possible use of such a half-bridge circuit, a possible interconnection of the half-bridge circuit in a switching regulator is depicted by dashed lines shown in Fig. 2. During the operation of the switching regulator, an input voltage U_{in} is applied to the connection terminals K1, K2, which is converted into an output voltage U_{out} present at output terminals AK1, AK2. To that end, a series circuit including a coil L and a capacitor C_{out} is connected in parallel with the drain-source path DN - SN of the n-channel transistor N. It is possible to tap off the output voltage U_{out} across the capacitor C_{out} . The ratio of input voltage U_{in} to output voltage U_{out} is dependent on the time durations during which the p-channel transistor P and the n-channel transistor N are alternately switched on. If the p-channel transistor P is in the on state, then the series circuit including the coil L and the capacitor C_{out} is connected to the input voltage U_{in} . If the p-channel transistor P is in the off state and the n-channel transistor N is in the on state,

then the n-channel transistor N closes the electric circuit between the inductor L and the capacitor Cout, the inductor L outputting the previously stored energy to the capacitor Cout.

5 In order to turn on the n-channel transistor N, a potential that is greater than the potential at the source connection SN is required at the gate connection GN. To that end, the gate connection GN is preferably connected to the first connection terminal K1. In order to turn off the n-channel transistor N, the gate connection GN is preferably connected to the second supply terminal K2 by the drive circuit 10. To turn on the p-channel transistor P, the gate connection GP is preferably connected to the second supply terminal K2 via the output 104 of the drive circuit 10. To turn off the p-channel transistor P, the gate connection GP thereof is preferably connected to the first supply terminal K1 via the output 104 of the drive circuit 10. No bootstrap circuit is required for driving the p-channel transistor P.

20 The two transistors P, N are designed as vertical power MOSFETs. Each of the two transistors are integrated in a respective semiconductor body CH1, CH2 with a front side and a rear side. The drain connections DP, DN of the two transistors P, N are available at the rear sides of the semiconductor bodies CH1, CH2. The drive circuit 10 is preferably integrated in a third semiconductor body with a front side and a rear

side, and the rear side of this third semiconductor body forms the connection 103 of the drive circuit.

Figs. 3a and 3b show an exemplary embodiment of the inventive half-bridge circuit, in which the two transistors P, N that are each integrated into a respective semiconductor body CH1, CH2 are arranged on a common connection plate 20. Fig. 3a shows the arrangement in plan view and Fig. 3b shows a lateral sectional illustration of the arrangement along the section line A-A' depicted in Fig. 3a.

The n-channel transistor N and the p-channel transistor P are in each case integrated in a semiconductor body or a chip CH1, CH2, which are each of essentially parallelepipedal design. In this case, a rear side CH1R of the semiconductor body CH1 of the n-channel transistor N forms the drain connection DN of the transistor N and a rear side CH2R of the semiconductor body CH2 of the p-channel transistor P forms the drain connection DP of the transistor. The two transistors N, P, or the semiconductor bodies CH1, CH2, are applied to the connection plate 20 next to one another by their rear sides CHR1, CH2R and are electrically conductively connected to the plate. Connecting layers 42, 44 between the semiconductor bodies CH1, CH2 and the connection plate 20 include, for example, an electrically conductive soldering material or an electrically conductive adhesive. In this way, the drain

connections DN, DP are electrically conductively connected to one another via the connecting layers 42, 44 and via the connection plate 20.

5 The source connection SN and the gate connection GN of the n-channel transistor N are available at the front side CH1V of the semiconductor body CH1. Correspondingly, the source connection SP and the gate connection GP of the p-channel transistor P are available at the front side CH2V of the semiconductor body CH2. In this case, the source connections SN, SP each occupy a large part of the areas of the front sides CH1V, CH2V. In the example illustrated, the gate connections GN, GP are each situated in a corner of the essentially square front sides CH1V, CH2V and are electrically insulated from the source connections SN, SP surrounding the gate connections GN, GP by insulation layers OX1, OX2. The gate connections GN, GP can be situated at virtually any other positions at the front sides CH1V, CH2V of the semiconductor bodies CH1, CH2. Thus, the gate connections GP, GN may be arranged, in particular, at the edge of the respective front side CHV1, CHV2 as shown by the solid lines in Fig. 3a or the gate connections GP, GN can be arranged in the center between two corners, as is illustrated by the broken lines in the semiconductor body CH1 shown in Fig. 3a.

The connection plate 20 with the transistors N, P arranged thereon is preferably surrounded by a plastic layer 50, in order to protect the transistors N, P against mechanical influences. This plastic layer 50 forms a housing 50, which is illustrated by the broken lines shown in Figs. 3a, 3b. The connection plate 20 has a connection pin 203 which projects from the housing 50 to enable external contact with the connection plate 20 and hence with the drain connections DN, DP of the two transistors P, N. Further electrically conductive connection pins 201, 202, 204, 205 which project from the housing 50 are provided on the housing 50. The connection pin 201 serves for making contact with the source connection SN of the first transistor N and is therefore connected to the source connection SN at the front side CH1V of the chip CH1 by a bonding wire B1. The connection pin 202 serves for making contact with the gate GN of the n-channel transistor N. The gate GN at the front side CH1V of the chip CH1 is therefore connected to the connection pin 202 by a bonding wire B2. In a corresponding manner, the gate GP at the front side CH2V of the chip CH2 is connected to the connection pin 204 by a bonding wire B3, and the source connection SP is connected to the connection pin 205 by a bonding wire B4. The connection pin 201 of the arrangement illustrated in Fig. 3a forms the connection terminal K2 of the circuit shown in Fig. 2. The connection pin 205 forms the connection terminal K1. The connection pin 202 forms the connection terminal for

connection of the second output 105 of the drive circuit 10,
which is not illustrated in greater detail in Fig. 3a. The
connection pin 204 forms the connection terminal for the first
output 104 of the drive circuit. The connection pin 203 of the
5 common connection plate 20 forms the output OUT of the half-
bridge circuit.

Fig. 4 shows a further exemplary embodiment of the half-bridge
circuit according to the invention, in which the drive circuit
10 is integrated in a semiconductor body CH3 or a chip CH3
which is applied directly to the front side CH1V of the
semiconductor body CH1. The input connection 101 for feeding
in the input signal SN, the connection 102 for connecting to
the terminal K1, the connection 103 for connecting to the
15 terminal 103, and the outputs 104, 105 of the drive circuit 10
are located at a front side CH3V of the drive circuit 10.

In the exemplary embodiment illustrated, the arrangement shown
in Fig. 4 is partly surrounded by a plastic layer. Five
20 connection legs 201, 202, 203, 204, 205 project from the
plastic layer. One of the connection legs 203 is part of the
connection plate 20 and forms the output OUT of the half-
bridge circuit.

25 The allocation of the connection legs shown in Fig. 4a differs
from that in Fig. 3a because the drive circuit 10 is

accommodated in the housing 50 and need not be connected via the connection legs to the transistors N, P. Thus, in the exemplary embodiment shown in Fig. 4a, the connection legs 201, 202 are provided for connecting to the second terminal or 5 actually form the second supply terminal K2. To that end, the source connection SN1 of the first transistor N is connected to the connection legs 201, 202 by two bonding wires B1, B2. Connection by means of the two bonding wires B1, B2 provides the advantage that the source SN of the transistor N is connected in a low-impedance manner to the terminal K2, or to the supply potential available there, usually ground. The source SP at the front side CH2V of the semiconductor body CH2 is connected to the connection leg 205 by a bonding wire B3; the connection layer forming the first terminal K1. Furthermore, the input connection 101 of the drive circuit 10 15 is connected to the connection leg 204 by a bonding wire B5; the connection layer forming the input connection 101 of the drive circuit for feeding in the input signal Sin.

20 Within the housing, the connection 102 of the drive circuit 10 is connected to the source SP of the p-channel transistor P by a bonding wire B6, and via the source SP and via the bonding wire B3, to the terminal K1. The first output 104 of the drive circuit 10 is connected to the gate GP on the chip CH2 by a 25 bonding wire B7, and the output 105 is connected to the gate GN on the chip CH1 of the n-channel transistor N by a bonding

wire B8. The connection 103 is connected by a bonding wire B9 to the source SN, and consequently, via the bonding wires B1, B2 to the connection legs 201, 202, which form the second terminal K2.

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As can be gathered from Fig. 4b, in particular, the rear side CH3R of the semiconductor body CH3 is applied to the front side CH1V of the first semiconductor body CH1.

10 Protective layers made of an imide are usually applied to the front sides CHV1, CHV2 of the semiconductor bodies CH1, CH2. The bonding wires B1, B2, B3, B9 for producing electrical contacts penetrate these protective layers. The protective layer applied to the front side CHV1 prevents the existence of
15 an electrical contact between the source SN at the front side CHV1 of the first semiconductor body CH1 and the rear side CH3R of the semiconductor body CH3. The task of the protective layer is to protect the semiconductor bodies CH1, CH2 from damage, in particular when the semiconductor body CH3 is
20 placed onto the semiconductor body CH1.

In the embodiment illustrated in Fig. 4c, such a protective layer is dispensed with at the front side CH1V of the semiconductor body CH1 and the rear side CH3R of the
25 semiconductor body CH3 forms the connection 103 of the drive circuit 10 for connecting to the terminal K2. The rear side

CH3R of the semiconductor body CH3 is applied to the source connection SN1 at the front side CH1V of the semiconductor body CH1 of the n-channel transistor N by an electrically conductive layer 46, for example, a soldering layer or an electrically conductive adhesive. The connection 103 of the drive circuit 10 and the source connection SN1 are electrically connected to one another by the electrically conductive layer 46. As a result, it is possible to dispense with a contact area for the connection 103 at the front side CH3V of the semiconductor body CH3 and the bonding wire B9.

The circuit arrangement shown in Figs. 4a-4c represents a space-saving realization of the half-bridge circuit, which is illustrated in the circuit diagram in Fig. 2, - with the drive circuit 10 and the transistors P, N.

Fig. 5 shows the circuit diagram of a further exemplary embodiment of an inventive half-bridge circuit, which differs from that illustrated in Fig. 2 by a capacitor Cb, which is connected to the connection terminals K1, K2.

Figs. 6a and b show a space-saving realization of the circuit arrangement shown in Fig. 5. The capacitor Cb is preferably designed as a ceramic multilayer capacitor having a parallelepipedal form. The connections of the parallelepipedal capacitor Cb are arranged at ends thereof.

In an embodiment that is not specifically illustrated, one of the connections is connected to the source region SN at the front side CHV1 of the chip CH1 of the n-channel transistor N by a bonding wire, and the other connection is electrically conductively connected to the source region SP at the front side CH2V of the chip CH2 by a bonding wire. It is necessary to connect the capacitor Cb to the source connections SN, SP by bonding wires when electrically insulating protective layers that are penetrated by the bonding wires are applied to the front sides CH1V, CH2V of the semiconductor bodies.

In the exemplary embodiment illustrated in Fig. 6b, no such protective layer is applied to the front sides CH1V, CH2V of the semiconductor bodies CH1, CH2. In this embodiment, one of the connections of the capacitor Cb is applied to the source region SN at the front side CH1V of the chip CH1 of the n-channel transistor N by an electrically conductive layer 47. The other connection is connected to the source region SP at the front side CH2V of the chip CH2 of the p-channel transistor P by an electrically conductive layer 49. The electrically conductive layers 47, 49 are preferably layers made of soldering material or layers made of electrically conductive adhesive.

The arrangement in accordance with Fig. 6 is also preferably enclosed by a plastic layer 50 forming a housing for the arrangement.